DECLARATION

I, the undersigned, of 2-12, Nakazaki 2-chome, Kita-ku, Osaka, Japan, hereby certify that I am well acquainted with the English and Japanese languages, that I am an experienced translator for patent matter, and that the attached document is a true English translation of

Japanese Patent Application No. **10-198269**

that was filed in Japanese.

I declare that all statements made herein of may own knowledge are true, that all statements on information and belief are believed to be true, and that these statements were made with the knowledge that willful statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Signature:

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Dated: **September 24, 2002**

[Name of the Document] SPECIFICATION

[Title of the Invention] SEMICONDUCTOR DEVICE

[Claims]

[Claim 1] A semiconductor device with a line structure formed on a semiconductor substrate, characterised in that

the line structure comprises:

a conductor layer formed on the semiconductor substrate;

a dielectric film formed on the conductor layer; and

a conductor line formed on the dielectric film,

the dielectric film comprises:

a first dielectric portion, at least part of the first dielectric portion being located between the lower surface of the conductor line and the upper surface of the conductor layer; and

second and third dielectric portions laterally arranged to interpose the first dielectric portion therebetween, and

the first dielectric portion has a dielectric constant different from at least one of the dielectric constants of the second and third dielectric portions.

[Claim 2] The semiconductor device of Claim 1, characterised in that the dielectric constant of the first dielectric portion is lower than those of the second and third dielectric portions.

[Claim 3] The semiconductor device of Claim 1 or 2, characterised in that at least one of the dielectric constants of the second and third dielectric portions is higher than 10.

[Claim 4] The semiconductor device of any one of Claims 1 through 3, characterised by further comprising another dielectric film covering the conductor line.

[Claim 5] The semiconductor device of any one of Claims 1 through 4, characterised by further comprising an active component operable at radio frequencies, the active component being formed on the semiconductor substrate and electrically connected to the line structure.

[Claim 6] A semiconductor device with a line structure formed on a semiconductor substrate, characterised in that

the line structure comprises:

a conductor layer formed on the semiconductor substrate;

a dielectric film formed on the conductor layer; and

a conductor line formed on the dielectric film, and

the dielectric film includes two or more dielectric layers with mutually different dielectric constants.

[Claim 7] The semiconductor device of Claim 6, wherein

at least one of the two or more dielectric layers comprises: a first dielectric portion, at least part of the first dielectric portion being located between the lower surface of the conductor line and the upper surface of the conductor layer; and second and third dielectric portions laterally arranged to interpose the first dielectric portion therebetween, and

the first dielectric portion has a dielectric constant different from at least one of the dielectric constants of the second and third dielectric portions.

[Claim 8] A semiconductor device with a line structure formed on a semiconductor substrate, characterised in that

the line structure comprises:

a conductor layer formed on the semiconductor substrate;

a dielectric film formed on the conductor layer;

a conductor line formed on the dielectric film; and

another dielectric film covering the conductor line.

[Claim 9] The semiconductor device of Claim 8, characterised in that the dielectric film includes two or more dielectric layers with mutually different dielectric constants.

[Claim 10] A semiconductor device with a line structure formed on a semiconductor substrate, wherein

the line structure comprises:

a conductor layer formed on the semiconductor substrate;

a dielectric film formed on the conductor layer; and

a conductor line formed on the dielectric film, and

a region of the conductor layer located under the conductor line is removed.

[Claim 11] The semiconductor device of Claim 10, characterised in that the dielectric film includes two or more dielectric layers with mutually different dielectric constants.

[Claim 12] The semiconductor device of Claim 10 or 11, characterised by further comprising a second dielectric film covering the conductor line.

[Claim 13] The semiconductor device of Claim 12, characterised in that the dielectric constant of the second dielectric film is higher than 10.

[Claim 14] The semiconductor device of any one of Claims 10 through 13, characterised by further comprising an active component operable at radio frequencies, the active component being formed

on the semiconductor substrate and electrically connected to the line structure.

[Claim 15] A semiconductor device with a line structure formed on a semiconductor substrate, wherein

the line structure comprises:

a coplanar conductor layer formed over the semiconductor substrate; and

a dielectric film formed on the coplanar conductor layer.

[Claim 16] The semiconductor device of Claim 15, characterised in that the dielectric constant of the dielectric film is 10 or more.

[Claim 17] The semiconductor device of Claim 15 or 16, characterised by further comprising an active component operable at radio frequencies, the active component being formed on the semiconductor substrate and electrically connected to the line structure.

[Claim 18] A semiconductor device with a line structure formed on a semiconductor substrate, wherein

the line structure comprises:

a first dielectric film formed on the semiconductor substrate;

a coplanar conductor layer formed on the first dielectric film; and

a second dielectric film formed on the coplanar conductor layer.

[Claim 19] The semiconductor device of Claim 18, characterised in that the dielectric constant of at least one of the first and second dielectric films is 10 or more.

[Claim 20] The semiconductor device of Claim 19, characterised in that the first dielectric film includes two or more dielectric layers with mutually different dielectric constants.

[Claim 21] The semiconductor device of any one of Claims 18 through 20, characterised by further comprising an active component operable at radio frequencies, the active component being formed on the semiconductor substrate and electrically connected to the line structure.

[Detailed Description of the Invention]

[Technical Field to which the Invention Belongs]

The present invention generally relates to a semiconductor device, and more particularly relates to a line structure for a semiconductor device operable at radio frequencies, which is suitable to downsizing and performance enhancement of mobile communications terminals.

[Prior Art]

In recent years, the applications of mobile communications equipment of various types, including portable telephones and portable data terminals, have been spanning a wider and wider range over the world. In Japan, cellular phones, operating on 900 MHz and 1.5 GHz bands, and personal handy phone systems (PHS), operating on 1.9 GHz band, have been popularised. Globally speaking, European GSM and DECT phones and American PCS phones are very popular.

Among these numerous types of mobile communications terminals, portable terminals, in particular, are required to be as small in size and as light in weight as possible. Thus,

first of all, components for a portable terminal should have its size reduced and its performance enhanced. For example, to downsize a transmitting power amplifier for use in a radio-frequency transmitter for a portable terminal (hereinafter, simply referred to as a "power amplifier"), it is strongly needed to implement the power amplifier as a monolithic microwave IC (MMIC) of GaAs. In an MMIC, active components, matching circuit and bias supply are all integrated on a single chip. Thus, an MMIC can more effectively contribute to downsizing than a hybrid IC (HIC), in which matching circuit and bias supply are implemented as discrete chip components.

From a viewpoint of performance enhancement, however, an MMIC is said to be inferior to an HIC. This is because if a power amplifier is implemented as an MMIC, for instance, then parasitic resistive components, such as interconnection resistance, which are involved with semiconductor device processing for fabricating the MMIC, adversely increase, thus causing a considerable loss of the power to be transmitted. For that reason, a power amplifier implemented as an MMIC often results in lower power gain, lower power amplification and deteriorated distortion characteristic compared to a power amplifier implemented as an HIC. Thus, according to the currently available techniques, it is determined based on a necessary trade-off between downsizing and performance enhancement which part of a power amplifier should be implemented as an MMIC.

Hereinafter, an exemplary MMIC implementation of output matching circuit and drain-biasing circuit will be described with

reference to Figures 10 through 15. An exemplary microstrip line structure will also be described with reference to Figure 16. A microstrip line structure is a basic structure of a spiral inductor used as a passive component in the output matching circuit and drain-biasing circuit.

Figure 10 illustrates a planar pattern for a final-stage MESFET and an output matching circuit thereof used for a high-output power amplifier transmitting a power of about 1 W. Following is respective parameters of the final-stage MESFET.

Unit finger length: 300 μm

Total gate width: 24 mm

Frequency: 900 MHz

Power supply voltage: 3.5 V

Saturated output power with idle current of 400 mA supplied: about 1.5 W

Operating current: about 550 mA

Gain: about 12 dB

The gate of the MESFET 410 is connected to a gate-biasing pad 412 via a gate electrode extended line 411. The source of the MESFET 410 is connected to an MIM capacitor 409 via a source pad 413. The drain of the MESFET 410 is connected to a drain-biasing pad 415 via a drain extended line 414. One terminal of a spiral inductor 408 is connected to a part of the drain extended line 414, while the other terminal thereof is connected to an output pad 416 via the MIM capacitor 409.

The line of the spiral inductor 408 is made of gold plate, and the thickness is of about 3 μm for example. The extended

lines thereof are formed by evaporating and depositing titanium and gold thereon. The upper-layer conductor of the MIM capacitor 409 is made of gold plated, while the lower-layer conductor thereof is formed by evaporating and depositing titanium and gold thereon. The interlayer dielectric film of the capacitor 409 is formed by depositing silicon nitride (SiN_x) with a dielectric constant of about 7 by a CVD process.

In the MMIC including the output matching circuit, the final-stage MESFET operates at a frequency of 900 MHz with a current of about 560 mA supplied. The MESFET provides a saturated output power of about 1.0 W with a power supply voltage of 3.5 V applied, and shows a gain of about 10 dB.

Figure 11 illustrates an equivalent circuit of the MESFET and output matching circuit thereof shown in Figure 10. A MESFET shown in Figure 11, including gate 302, source 303 and drain terminals 304, corresponds to the MESFET 410 shown in Figure 10. Equivalent series inductor 305, equivalent series resistor 306 and equivalent parallel capacitor 307 are connected to the drain terminal 304 of the MESFET. The equivalent series indictor 305 and resistor 306 form an equivalent circuit of the spiral inductor 408. In this example, the inductance value of the equivalent series inductor 305 is about 2.5 nH, the resistance value of the equivalent series resistor 306 is about 4Ω and the capacitance value of the equivalent parallel capacitor 307 is about 12 pF. The equivalent parallel capacitor 307 corresponds to the MIM capacitor 409 shown in Figure 10.

Figure 12 illustrates a location of load impedance Z_L 301

of the MESFET on a Smith chart showing impedance matching from a 50Ω line. The load impedance Z_L 301 can be impedance-matched with the centre of the Smith chart at 50Ω by tracing paths formed by the parallel capacitive components and series inductive components. In this case, the value of the load impedance Z_L 301 is 7Ω+j4Ω.

Next, a drain-biasing circuit and a MESFET, in which a drain choking inductor is implemented as a part of an MMIC, will be described with reference to Figure 13. The choking inductor is a device used for preventing radio frequency power from leaking to the drain power supply.

Following is respective parameters of the MESFET.

Unit finger length: 100μm

Total gate width: 1 mm

Frequency: 900 MHz

Power supply voltage: 3.5 V

Saturated output power with idle current of 20 mA supplied: about 120 mW

Operating current: about 23 mA

Gain: about 13 dB

The gate of the MESFET 505 is connected to a gate-biasing pad 507 via a gate electrode extended line 506. The source of the MESFET 505 is connected to a source pad 508. The drain of the MESFET 505 is connected to a drain extended line 509. Part of the drain extended line 509 is connected to a drain-biasing pad 510 via a spiral inductor 504.

In the MMIC including the drain choking inductor, the MESFET

operates at a frequency of 900 MHz and with a power supply voltage of 3.5 V applied and a current of about 19 mA supplied. The MESFET provides a saturated output power of about 90 mW with an idle current of 20 mA supplied, and shows a gain of about 11 dB.

The line of the spiral inductor 504 is made of gold plate, and the thickness is of about 3 μm. The extended lines thereof are formed by evaporating and depositing titanium and gold thereon.

Figure 14 illustrates an equivalent circuit of the MESFET 505 and the drain-biasing circuit shown in Figure 13. An equivalent series inductor 502 and an equivalent series resistor 503 constitute an equivalent circuit of the spiral inductor 504 shown in Figure 13. In this example, the inductance value of the equivalent series inductor L 502 is 21 nH and the resistance value of the equivalent series resistor R 503 is 7.5Ω.

Figure 15 illustrates the location of choke impedance Z_c 501 on a Smith chart. The choke impedance is located at a drain terminal of the MESFET, which is short-circuited at an end through which a drain voltage is applied. Usually, the choke impedance Z_c 501 is ideally defined to be open. But since the choke impedance is sometimes used as a matching circuit in practice, the choke impedance is not necessarily open. In the example shown in Figure 15, the choke impedance Z_c 501 is located at an angle of phase rotation of about 140 degrees.

Figure 16 illustrates the cross section of a microstrip line structure, which is a basic structure of a spiral inductor. As described above, a spiral inductor is used as a passive component for an output matching circuit or a drain-biasing circuit. Such

a line structure includes: a line 602 formed on the surface of a GaAs substrate 601; and a grounded conductor 603 formed on the back of the GaAs substrate 601. The line 602 may be made of gold plated to be about 3μm thick for example.

[Problems that the Invention is to solve]

In the first prior art example illustrated in Figures 10 through 12, the output impedance of the final-stage GaAs FET used as a power amplifier is as low as about 10Ω or less. Accordingly, the resistive components of the output matching circuit, including the interconnection resistance of the spiral inductor formed on the GaAs substrate, increases the power lost by the output matching circuit. As a result, the power amplifier shows lower gain, lower power amplification (corresponding to operating current) and deteriorated distortion characteristic. In order to avoid problems such as these, the thickness or width of a line may be increased. However, the thickness of a line cannot exceed a certain upper limit defined by various restrictions on semiconductor device processing. Also, the wider a line, the larger the area occupied by the line on a chip, which is contradictory to the demand of downsizing.

Even in a medium-output power amplifier transmitting a power of about 100 W, the input, interstage and output matching circuits thereof are included in an MMIC. In such a case, the output matching circuit is built in an MMIC, in which the output impedance of a final-stage GaAs FET used for the power amplifier is as high as approximately 300Ω or more. Even so, the resistive components of the output matching circuit, including the interconnection resistance of the spiral inductor formed on the GaAs substrate,

increases the power lost by the output matching circuit, thus adversely affecting the performance thereof.

In the second prior art example shown in Figures 13 through 15, since the drain-biasing circuit is implemented as a part of an MMIC, the choking spiral inductor occupies a larger area on a GaAs substrate, thereby increasing the area of the MMIC chip and interfering with downsizing. Furthermore, a drain voltage externally applied drops due to the parasitic resistance of the spiral inductor line, resulting in deterioration in performance of the power amplifier. Accordingly, the second prior art example cannot make full use of the essential characteristics of the power amplifier, and cannot sufficiently contribute to the performance enhancement thereof.

The present invention has been made in view of the above problems, and therefore an object of the present invention is providing a semiconductor device operable at radio frequencies, which can contribute to both downsizing and performance enhancement of mobile communications terminals.

[Means for Solving the Problems]

A semiconductor device according to the present invention has a line structure formed on a semiconductor substrate, and is characterised in that the line structure includes: a conductor layer formed on the semiconductor substrate; a dielectric film formed on the conductor layer; and a conductor line formed on the dielectric film, the dielectric film includes: a first dielectric portion, at least part of the first dielectric portion being located between the lower surface of the conductor line and the upper surface

of the conductor layer; and second and third dielectric portions laterally arranged to interpose the first dielectric portion therebetween, and the first dielectric portion has a dielectric constant different from at least one of the dielectric constants of the second and third dielectric portions.

In one embodiment of the present invention, the dielectric constant of the first dielectric portion may be lower than those of the second and third dielectric portions.

At least one of the dielectric constants of the second and third dielectric portions is preferably higher than 10.

The semiconductor device preferably further includes another dielectric film covering the conductor line.

In another embodiment of the present invention, the semiconductor device may further include an active component operable at radio frequencies, the active component being formed on the semiconductor substrate and electrically connected to the line structure.

Another semiconductor device according to the present invention has a line structure formed on a semiconductor substrate, and is characterised in that the line structure includes: a conductor layer formed on the semiconductor substrate; a dielectric film formed on the conductor layer; and a conductor line formed on the dielectric film, and the dielectric film includes two or more dielectric layers with mutually different dielectric constants.

In this semiconductor device, at least one of the two or more dielectric layers may include: a first dielectric portion, at least

part of the first dielectric portion being located between the lower surface of the conductor line and the upper surface of the conductor layer; and second and third dielectric portions laterally arranged to interpose the first dielectric portion therebetween. The first dielectric portion may have a dielectric constant different from at least one of the dielectric constants of the second and third dielectric portions.

Still another semiconductor device according to the present invention also has a line structure formed on a semiconductor substrate, and is characterised in that the line structure includes: a conductor layer formed on the semiconductor substrate; a dielectric film formed on the conductor layer; a conductor line formed on the first dielectric film; and a second dielectric film covering the conductor line.

In this semiconductor device, the dielectric film preferably includes two or more dielectric layers with mutually different dielectric constants.

Yet another semiconductor device according to the present invention also has a line structure formed on a semiconductor substrate, the line structure includes: a conductor layer formed on the semiconductor substrate; a dielectric film formed on the conductor layer; and a conductor line formed on the dielectric film, and a region of the conductor layer located under the conductor line is removed.

In this semiconductor device, the dielectric film preferably includes two or more dielectric layers with mutually different dielectric constants.

The above semiconductor device preferably further includes a second dielectric film covering the conductor line.

The dielectric constant of the second dielectric film is preferably higher than 10.

In another embodiment, the semiconductor device may further include an active component operable at radio frequencies, the active component being formed on the semiconductor substrate and electrically connected to the line structure.

Yet another semiconductor device according to the present invention also has a line structure formed on a semiconductor substrate, and the line structure includes: a coplanar conductor layer formed over the semiconductor substrate; and a dielectric film formed on the coplanar conductor layer.

In this semiconductor device, the dielectric constant of the dielectric film is preferably 10 or higher.

In one embodiment, the semiconductor device is characterised by further including an active component operable at radio frequencies, the active component being formed on the semiconductor substrate and electrically connected to the line structure.

Yet another semiconductor device according to the present invention also has a line structure formed on a semiconductor substrate, and the line structure includes: a first dielectric film formed on the semiconductor substrate; a coplanar conductor layer formed on the first dielectric film; and a second dielectric film formed on the coplanar conductor layer.

The dielectric constant of at least one of the first and

second dielectric films is preferably 10 or higher.

The first dielectric film preferably includes two or more dielectric layers with mutually different dielectric constants.

In another embodiment, the semiconductor device may further include an active component operable at radio frequencies, the active component being formed on the semiconductor substrate and electrically connected to the line structure.

[Embodiments of the Invention]

Hereinafter, preferred embodiments of a semiconductor device according to the present invention will be described with reference to the accompanying drawings.

(EMBODIMENT 1)

A first embodiment of a semiconductor device according to the present invention will be described with reference to Figures 1 through 3.

Figure 1 illustrates the cross section of a novel line structure applicable to the semiconductor device of the present invention. As shown in Figure 1, this line structure includes: a grounded conductor layer 102 (about 0.7 μm thick) made up of plural pairs of titanium and gold layers alternately stacked on the surface of a GaAs substrate 101; and a gold-plated line (conductor line) 105 provided over the grounded conductor layer 102 to be spaced apart therefrom. A dielectric film of about 0.1 μm to about 2 μm thick is formed on the grounded conductor layer 102. The dielectric film includes: a strontium titanate ($SrTiO_3$ or STO) layer 103; and a dielectric 104 of silicon nitride (SiN_x). In this embodiment, the SiN_x dielectric 104 is approximately as thick as the strontium titanate

layer 103, is in contact with the lower surface of the line 105 and is located in a region between the lower surface of the line 105 and the upper surface of the grounded conductor layer 102. In other words, the SiN_x dielectric 104 is laterally sandwiched by the strontium titanate layer 103. The dielectric constant of the SiN_x dielectric 104 is in the range from about 6 to about 7, which is much lower than that of the strontium titanate layer 103 in the range from about 50 to about 200.

An active component operable at radio frequencies, like a MESFET as described in the background section, is actually formed on the GaAs substrate 101, but is not shown in Figure 1 for the sake of simplicity. The line structure shown in Figure 1 is used for forming the spiral inductor shown in Figure 10 or 13, and is electrically connected to the RF active component and so on.

Hereinafter, a method for forming the line structure will be described with reference to Figures 2(a) through 2(f).

First, as shown in Figure 2(a), the grounded conductor layer 102, made up of titanium and gold layers alternately stacked, is deposited on the GaAs substrate 101 by a thin film deposition technique like evaporation. The thickness of the grounded conductor layer 102 is defined, for example, within the range from 0.5 μm to 3 μm. The material for the grounded conductor layer 102 is not necessarily limited to titanium and gold, but may be platinum (Pt) and tungsten silicon nitride (WSiN).

Next, as shown in Figure 2(b), the strontium titanate layer 103 (thickness: 1.5 μm) with a dielectric constant of about 100 is deposited on the grounded conductor layer 102 by RF sputtering.

Thereafter, a resist 106 is applied onto the strontium titanate layer 103, and then exposed to radiation and developed by a photolithographic process, so that an opening 107 with a width 108 of about 10μm is formed in the resist 106. The planar layout of the opening 107 is defined so as to correspond to that of the line 105 to be formed during a subsequent process step.

Then, as shown in Figure 2(c), portion of the strontium titanate layer 103 exposed inside the opening 107 is etched away, for example, by an ion milling technique, so that a recess (opening) 109 with a width substantially equal to the width 108 of the opening 107 is formed in the strontium titanate layer 103. This etching process is performed so as to expose the surface of the grounded conductor layer 102 at the bottom of the recess 109.

Subsequently, in this embodiment, as shown in Figure 2(d), a silicon nitride portion (SiN_x dielectric) 104 (thickness: 1.5 μm) with a dielectric constant of about 7 is formed within the recess (opening) 109 of the strontium titanate layer 103 by a thin film deposition technique such as a plasma CVD process. The silicon nitride portion 104 may be formed by a lift-off technique for example.

Thereafter, as shown in Figure 2(e), the gold-plated line 105 is formed on the dielectric 104. In this embodiment, the thickness of the line 105 is 3μm, the width 110 thereof is 15 μm, and the centreline of the SiN_x dielectric 104 is substantially aligned with that of the line 105. It should be noted that the centreline of the SiN_x dielectric 104 does not have to be aligned with that of the line 105. That is to say, the line 105 may partially overlap with the SiN_x dielectric 104 in the planar layout. In such

a case, since the equivalent dielectric constant of the dielectric film is set at an appropriate level, the length of the line required for realising desired impedance matching can be considerably shortened.

Figure 3(a) illustrates an equivalent circuit diagram where a spiral inductor such as that shown in Figure 13 is formed to have the line structure just described. Figure 3(b) illustrates respective angles of phase rotation for a microstrip line with the structure just described and for the conventional microstrip line structure shown in Figure 16 (hereinafter, simply referred to as a "conventional structure"). In the example illustrated in Figure 3(b), the lengths of these two types of lines are supposed to be equal to each other. Each of these angles of phase rotation represents a phase angle of an associated line on a Smith chart, where the far end of the line is short-circuited. And each angle can be used as an index for estimating a length of a line required for attaining desired impedance matching. More specifically, the larger the angle of phase rotation of a line, the shorter that portion of the line required for realising desired impedance matching. As can be seen from Figure 3(b), the angle of phase rotation of the line structure according to this embodiment is about 68 degrees larger than that of the conventional structure of the same length. Thus, according to the present invention, the required line length can be shortened compared to the conventional structure. This is because the equivalent dielectric constant of the dielectric film can be optimised by making up the dielectric film of plural parts with mutually different dielectric constants.

By using such a line structure, the line length of a spiral inductor required for matching the impedance of an active component with a desired load impedance or attaining a desired choke inductance can be shortened, thus reducing the parasitic resistive components involved with the spiral inductor. As a result, it is possible to provide a semiconductor device operable at radio frequencies and contributing to both downsizing and performance enhancement of mobile communications terminals.

It should be noted that if another strontium titanate film 111 is deposited to cover the strontium titanate layer 103 and the line 105 as shown in Figure 2(f), then the angle of phase rotation can be further increased. This is because the electrical length can be further shortened by covering the line with a dielectric film having a high dielectric constant.

At least half of the strontium titanate layer 103, sandwiching the SiN_x dielectric 104 on right- and left-hand sides, preferably has a dielectric constant higher than 10. This is because setting the dielectric constant of that portion at 10 or more can drastically reduce the electrical length. Examples of such films with high dielectric constants include a barium strontium titanate (BST) film, as well as a strontium titanate film.

Also, the dielectric film may have a multilayer structure including a first dielectric layer and a second dielectric layer formed on the first dielectric layer. In such a case, the dielectric constant of the first dielectric layer may be either higher or lower than that of the second dielectric layer. By employing this multilayer structure, the equivalent dielectric constant of the

dielectric film can be controlled at an appropriate value. Furthermore, after an opening has been provided only in the second dielectric layer, the opening may be filled in with a dielectric having a dielectric constant different from that of the second dielectric layer, and a line may be formed to overlap with silicon nitride. For example, an opening may be formed only in a second dielectric layer of strontium titanate and then filled in with silicon nitride. In such a case, the equivalent dielectric constant of the dielectric film can be controlled at a desired level even more easily.

(EMBODIMENT 2)

A second embodiment of a semiconductor device according to the present invention will be described with reference to Figures 4 through 6.

Figure 4 illustrates the cross section of a novel line structure applicable to the semiconductor device of the present invention. As shown in Figure 4, this line structure includes: a grounded conductor layer 202 (thickness: about 0.7 μm) made up of plural pairs of titanium and gold layers alternately stacked on the surface of a GaAs substrate 201; and a gold-plated line 204 provided over the grounded conductor layer 202 to be spaced apart therefrom. A strontium titanate ($SrTiO_3$) layer 203 about 0.1 μm to about 2 μm thick is formed on the grounded conductor layer 202. A portion of the grounded conductor layer 202 just under the line 204 has been removed, which is totally different from the line structure of the first embodiment. An RF active component, like a MESFET as described in the background section, is actually formed on the GaAs substrate 101, but is not shown in Figure 4 for the sake of simplicity.

Hereinafter, a method for forming the line structure will be described with reference to Figures 5(a) through 5(d).

First, as shown in Figure 5(a), the grounded conductor layer 202, made up of titanium and gold layers alternately stacked, is deposited on the GaAs substrate 201 by a thin film deposition technique like evaporation. Then, part of the grounded conductor layer 202, which is located just under the region where the line 204 is to be formed, is etched away. To shape the grounded conductor layer 202 into such a pattern, an unshown resist pattern may be defined on the grounded conductor layer 202 and then a portion of the grounded conductor layer 202, which is not covered with the resist pattern, may be removed by an ion milling technique for example. In this manner, an opening 205 with a width of about 10 μm is provided in the grounded conductor layer 202. The thickness of the grounded conductor layer 202 is defined, for example, within the range from about 0.5 μm to about 3 μm. The grounded conductor layer 202 is not necessarily made of titanium and gold, but may be made of platinum (Pt) and tungsten silicon nitride.

Next, as shown in Figure 5(b), the first strontium titanate layer 203 (thickness: 1.5 μm) with a dielectric constant of about 100 is deposited on the grounded conductor layer 202 by RF sputtering.

Thereafter, as shown in Figure 5(c), the gold-plated line 204 is formed on the first strontium titanate layer 203. In this embodiment, the thickness of the line 204 is 3 μm, the width 206 thereof is 15 μm, and the centreline of the region where the grounded conductor layer 202 does not exist (i.e., the opening 205) is substantially aligned with that of the line 204.

Subsequently, as shown in Figure 5(d), the second strontium titanate layer 207 is deposited over the first strontium titanate layer 203 to cover the line 204.

Figure 6 illustrates respective angles of phase rotation for a microstrip line with the structure just described and for the microstrip line structure (conventional structure) shown in Figure 16. In the example illustrated in Figure 6, the lengths of these two types of lines are supposed to be equal to each other. Each of these angles of phase rotation represents a phase angle of an associated line on a Smith chart, where the far end of the line is short-circuited. And the angle can be used as an index for estimating a line length required for attaining desired impedance matching. More specifically, the larger the angle of phase rotation of a line, the shorter that portion of the line required for realising desired impedance matching. As can be seen from Figure 6, the angle of phase rotation of the line structure according to this embodiment is about 116 degrees larger than that of the conventional structure of the same length. Accordingly, the line length can be shortened according to the present invention compared to the conventional structure. This is because the conventional structure requires a line length, which is longer than that required by the inventive structure by a quantity corresponding to the angle of phase rotation of 116 degrees, for attaining desired impedance matching.

By using such a line structure, the line length of a spiral inductor required for matching the impedance of an active component with a desired load impedance or attaining a desired choke inductance can be shortened, thus reducing the parasitic resistive components

involved with the spiral inductor. As a result, it is possible to provide a semiconductor device operable at radio frequencies and contributing to both downsizing and performance enhancement of mobile communications terminals.

The second strontium titanate layer 207, covering the line 204, preferably has a dielectric constant higher than 10. This is because the electrical length can be reduced even more drastically by covering the line with a film having a high dielectric constant. Examples of such films with high dielectric constants include a BST film, as well as a strontium titanate film.

Also, the dielectric film provided between the grounded conductor layer 202 and the line 204 may have a multilayer structure including a first dielectric layer and a second dielectric layer formed on the first dielectric layer. In such a case, the dielectric constant of the first dielectric layer may be either higher or lower than that of the second dielectric layer.

(EMBODIMENT 3)

A third embodiment of a semiconductor device according to the present invention will be described with reference to Figures 7 through 9.

Figure 7 illustrates the cross section of a novel line structure applicable to the semiconductor device of the present invention. A first strontium titanate layer 303 is provided on a GaAs substrate 301, a grounded conductor layer 302 and a line 305 each made of gold plate are provided on the first strontium titanate layer 303, and a second strontium titanate layer 304 is formed in a region covering the grounded conductor layer 302 and the line 305. Here, a structure

combining the grounded conductor layer 302 and the line 305 shall be called a "coplanar structure".

As shown in Figure 7, this line structure includes: the first strontium titanate layer 303 formed on the surface of a GaAs substrate 301; a grounded conductor layer 302 (about 0.7 μm thick) and a line 305 (about 0.7 μm thick), which are both made of gold plated to be about 0.7 μm thick on the first strontium titanate layer 303; and a second strontium titanate layer 304 formed to cover the grounded conductor layer 302 and the line 305. In this specification, the combination of the grounded conductor layer 302 and the line 305 will be called a "coplanar structure". A gap is provided between the line 305 and the grounded conductor layer 302.

An RF active component, like a MESFET as described in the background section, is actually formed on the GaAs substrate 301, but is not shown in Figure 7 for the sake of simplicity.

Hereinafter, a method for forming the line structure will be described with reference to Figures 8(a) through 8(c).

First, as shown in Figure 8(a), the strontium titanate layer 303 (thickness: 1.5 μm) with a dielectric constant of about 100 is deposited on the GaAs substrate 301 by RF sputtering.

Next, as shown in Figure 8(b), a conductor film (thickness: 3 μm), made up of titanium and gold layers alternately stacked, is deposited on the strontium titanate layer 303 by a thin film deposition technique like evaporation. The thickness of the conductor film is defined, for example, within the range from about 0.5 μm to about 6 μm. Then, the conductor film is patterned by lithography and etching processes, thereby forming the grounded

conductor layer 302 and the line 305 (the width 306 of which is at 15μm) at the same time. In this embodiment, the width of the space 307 between the line 305 and the grounded conductor layer 302 is also defined at about 15μm. The material of the conductor film is not limited to titanium and gold, but may be plated gold or aluminium (Al). The width of the space 307 is not necessarily 15μm, but may be appropriately selected within the range from about 5μm to about 100μm.

Subsequently, as shown in Figure 8(c), the strontium titanate layer 304 (thickness: 1.5μm) with a dielectric constant of about 100 is deposited by RF sputtering to cover the grounded conductor layer 302 and the line 305.

Figure 9 illustrates respective angles of phase rotation for a microstrip line with the structure just described and for the microstrip structure (conventional structure) shown in Figure 16. In the example illustrated in Figure 9, the lengths of these two types of lines are supposed to be equal to each other. Each of these angles of phase rotation represents a phase angle of an associated line on a Smith chart, where the far end of the line is short-circuited. And each angle can be used as an index for estimating a line length required for attaining desired impedance matching. More specifically, the larger the angle of phase rotation of a line, the shorter that portion of the line required for realising desired impedance matching. As can be seen from Figure 9, the angle of phase rotation of the line structure according to this embodiment is about 106 degrees larger than that of the conventional structure of the same length. Accordingly, the line length can be shortened

according to the present invention compared to the conventional structure.

By using such a line structure, the line length of a spiral inductor required for matching the impedance of an active component with a desired load impedance or attaining a desired choke inductance can be shortened, thus reducing the parasitic resistive components involved with the spiral inductor. As a result, it is possible to provide a semiconductor device operable at radio frequencies and contributing to both downsizing and performance enhancement of mobile communications terminals.

The first dielectric film, provided between the substrate 301 and both the grounded conductor layer 305 and the line 304, and the second dielectric film, covering the grounded conductor layer 305 and the line 304, preferably have a dielectric constant higher than 10. This is because the electrical length can be reduced even more drastically by covering the line with a dielectric film having a high dielectric constant. Examples of such films with high dielectric constants include a BST film, as well as a strontium titanate film.

Also, the first dielectric film, provided between the substrate 301 and both the grounded conductor layer 305 and the line 304, may have a multilayer structure including a first dielectric layer and a second dielectric layer formed on the first dielectric layer. In such a case, the dielectric constant of the first dielectric layer may be either higher or lower than that of the second dielectric layer.

[Effects of the Invention]

According to the present invention, the equivalent dielectric constant of a dielectric film can be optimised. In addition, the line length of a spiral inductor, which is required for matching the impedance of an active component with a desired load impedance or attaining a desired choke inductance, can be shortened, thereby reducing the parasitic resistive components involved. As a result, it is possible to provide a semiconductor device operable at radio frequencies and contributing to both downsizing and performance enhancement of mobile communications terminals.

[Brief Description of the Drawings]

[Fig. 1]

A cross-sectional view of a line structure for use in a semiconductor device according to a first embodiment of the present invention.

[Fig. 2]

(a) through (f) cross-sectional views illustrating respective process steps for forming the semiconductor device of the first embodiment.

[Fig. 3]

(a) illustrates an equivalent circuit of the line structure of the first embodiment; and (b) is a Smith chart illustrating respective angles of phase rotation for a microstrip line structure formed by the line structure shown in Figure 1 and a microstrip line structure shown in Figure 16.

[Fig. 4]

A cross-sectional view of a line structure for use in a semiconductor device according to a second embodiment of the present invention.

[Fig. 5]

(a) through (d) are cross-sectional views illustrating respective process steps for forming the semiconductor device of the second embodiment.

[Fig. 6]

A Smith chart illustrating respective angles of phase rotation for a microstrip line structure formed by the line structure shown in Figure 4 and the microstrip line structure shown in Figure 16.

[Fig. 7]

A cross-sectional view of a line structure for use in a semiconductor device according to a third embodiment of the present invention.

[Fig. 8]

(a) through (c) are cross-sectional views illustrating respective process steps for forming the semiconductor device of the third embodiment.

[Fig. 9]

A Smith chart illustrating respective angles of phase rotation for a microstrip line structure formed by the line structure shown in Figure 7 and the microstrip line structure shown in Figure 16.

[Fig. 10]

A plan view illustrating a final-stage MESFET and an output

matching circuit thereof used for a high-output power amplifier transmitting a power of about 1 Ẇ.

[Fig. 11]

An equivalent circuit diagram of the MESFET and output matching circuit thereof shown in Figure 10.

[Fig. 12]

A Smith chart illustrating a location of load impedance Z_L 301 of the MESFET shown in Figure 11 and showing impedance matching from a 50Ω line.

[Fig. 13]

A plan view illustrating a MESFET and a drain-biasing circuit thereof.

[Fig. 14]

An equivalent circuit diagram of the MESFET and drain-biasing circuit thereof shown in Figure 13.

[Fig. 15]

A Smith chart illustrating impedance at a drain terminal of the MESFET, which is short-circuited at an end through which a drain voltage is applied.

[Fig. 16]

A cross-sectional view illustrating a microstrip line structure, which is a basic structure of a conventional spiral inductor.

[Explanation of Reference Characters]

101 GaAs substrate 101

102 grounded conductor layer

103 strontium titanate layer

104 silicon nitride

105 line

106 resist

107 resist opening

108 opening width

109 opening

110 line width

111 second strontium titanate film

201 GaAs substrate

202 grounded conductor layer

203 strontium titanate layer ($SrTiO_3$ or STO)

204 line

205 opening

206 line width

207 second strontium titanate layer 207

301 GaAs substrate

302 grounded conductor layer

303 first strontium titanate layer

304 second strontium titanate layer

305 line

306 line width

307 space

401 load impedance Z_L

402 gate terminal

403 source terminal

404 drain terminal

405 equivalent series inductance L

406 equivalent series resistance R

407 equivalent parallel capacitance C

408 spiral inductor

409 MIM capacitor

410 MESFET

411 gate electrode extended line

412 gate-biasing pad

413 source pad

414 drain extended line

415 drain pad

416 output pad

501 choke impedance Z_c

502 equivalent series inductance L

503 equivalent series resistance R

504 spiral inductor

505 MESFET

506 gate electrode extended line

507 gate-biasing pad

508 source pad

509 drain extended line

510 drain pad

511 matching circuit

601 GaAs substrate

602 line

603 grounded conductor

[Name of the Document] ABSTRACT

[Abstract]

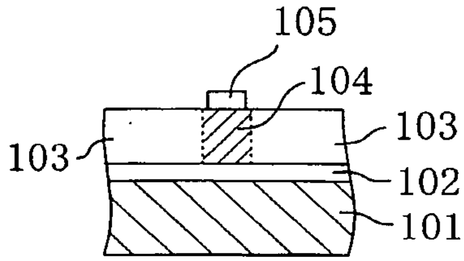
[Purpose] To provide a semiconductor device operable at radio frequencies, which can contribute to both downsizing and performance enhancement of mobile communications terminals.

[Solution] In a semiconductor device with a line structure formed on a GaAs substrate 101, the line structure includes a grounded conductor layer 102, a dielectric film and a conductor line 105, which are formed on the substrate 101. The dielectric film is composed of: a first dielectric portion (silicon nitride 104) located between the lower surface of the conductor line 105 and the upper surface of the conductor layer 102; and the other portion (strontium titanate film 103). The first dielectric portion has a dielectric constant different from that of the other portion, thereby optimising the equivalent dielectric constant of the dielectric film.

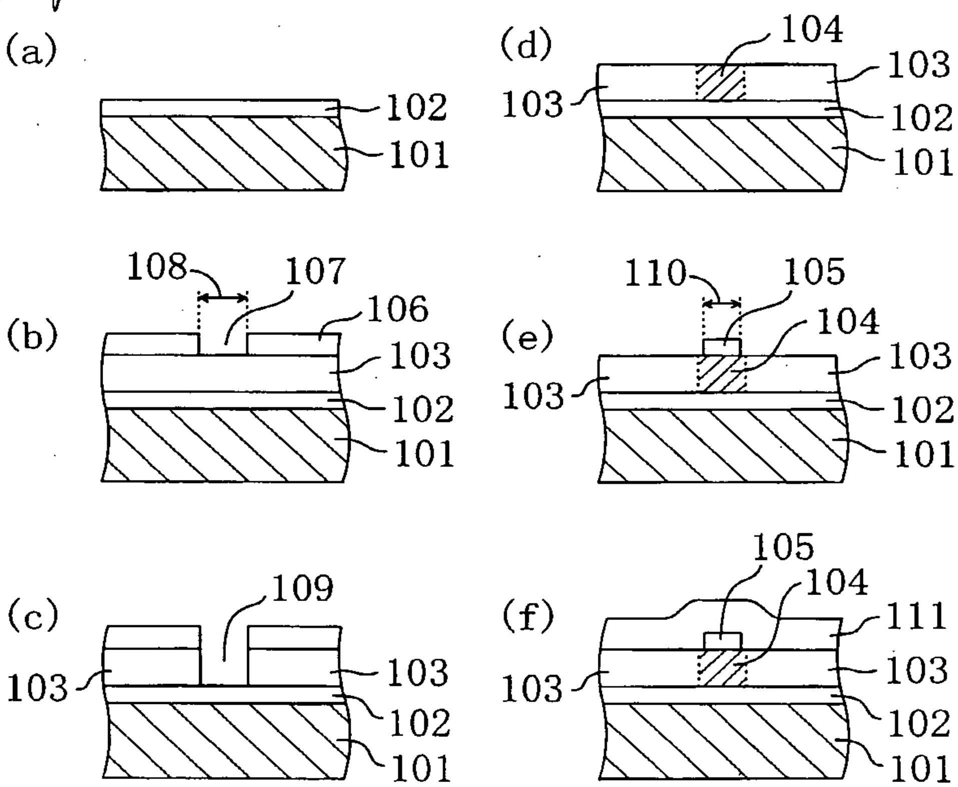
[Selected Figure] Figure 1

【書類名】 図面
[Name of the Document] DRAWINGS

【図１】
[Fig. 1]



【図２】
[Fig. 2]

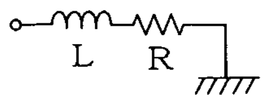


【図３】
[Fig. 3]

（a）

REFLECTION COEFFICIENT

S_{11}(反射係数)



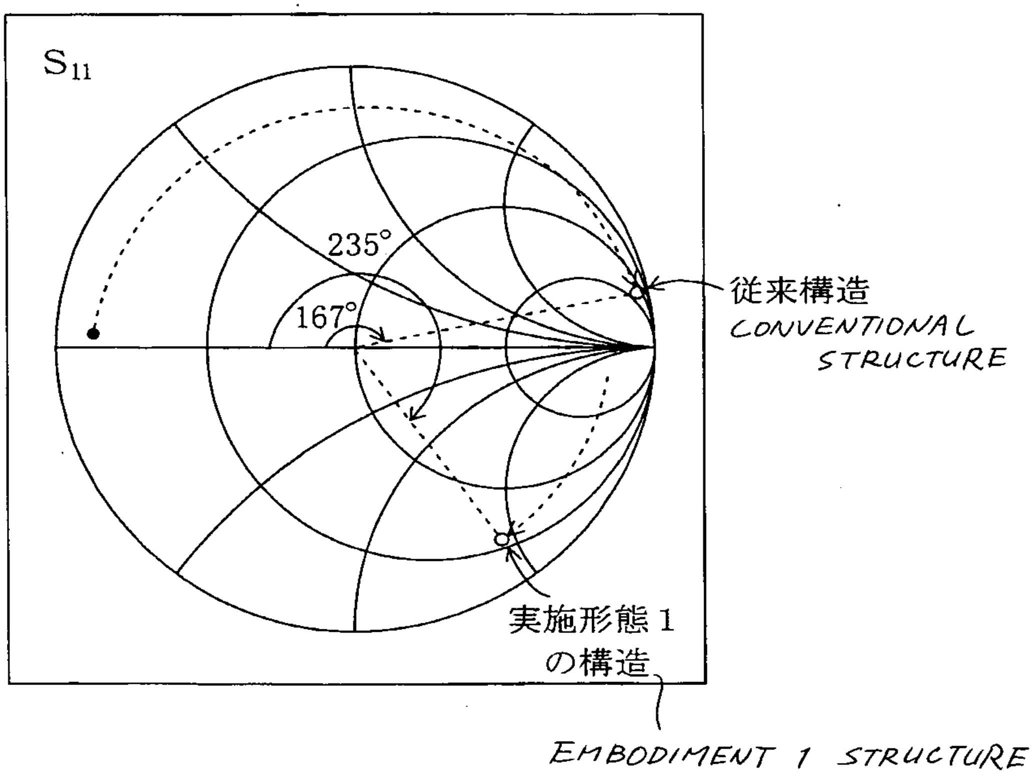
EQUIVALENT INDUCTANCE

L ：等価インダクタンス値

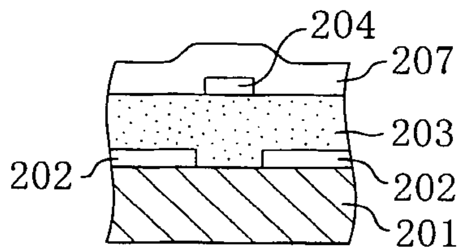
R ：等価抵抗値

EQUIVALENT RESISTANCE

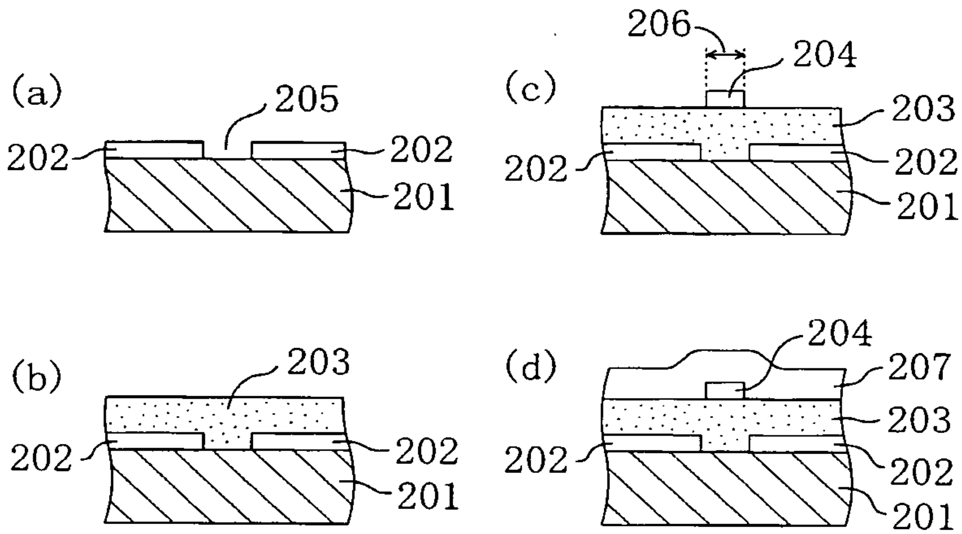
（b）



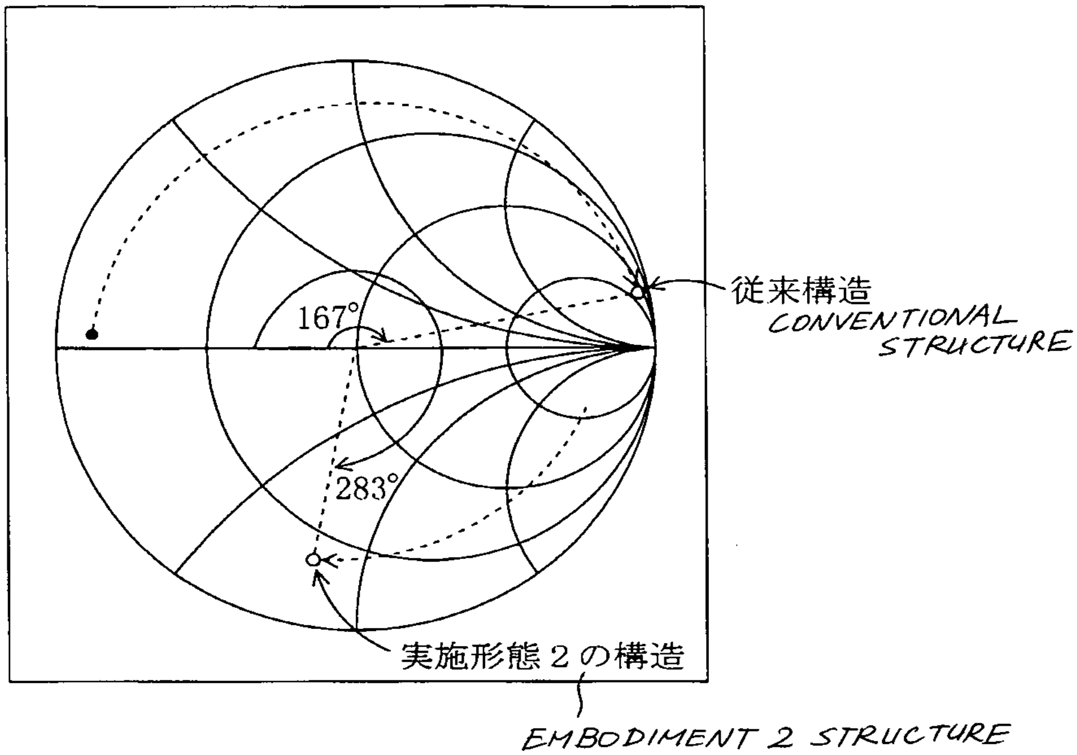
【図４】
[Fig. 4]



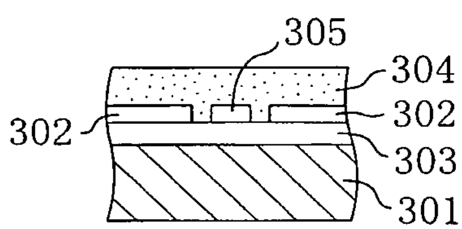
【図５】
[Fig. 5]



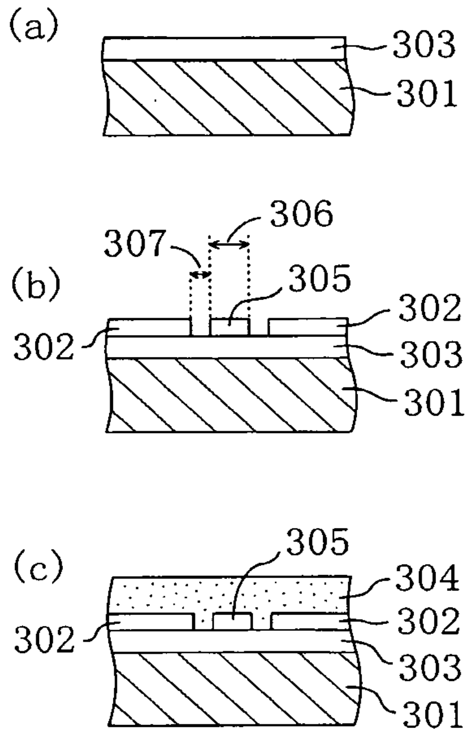
【図６】
[Fig. 6]



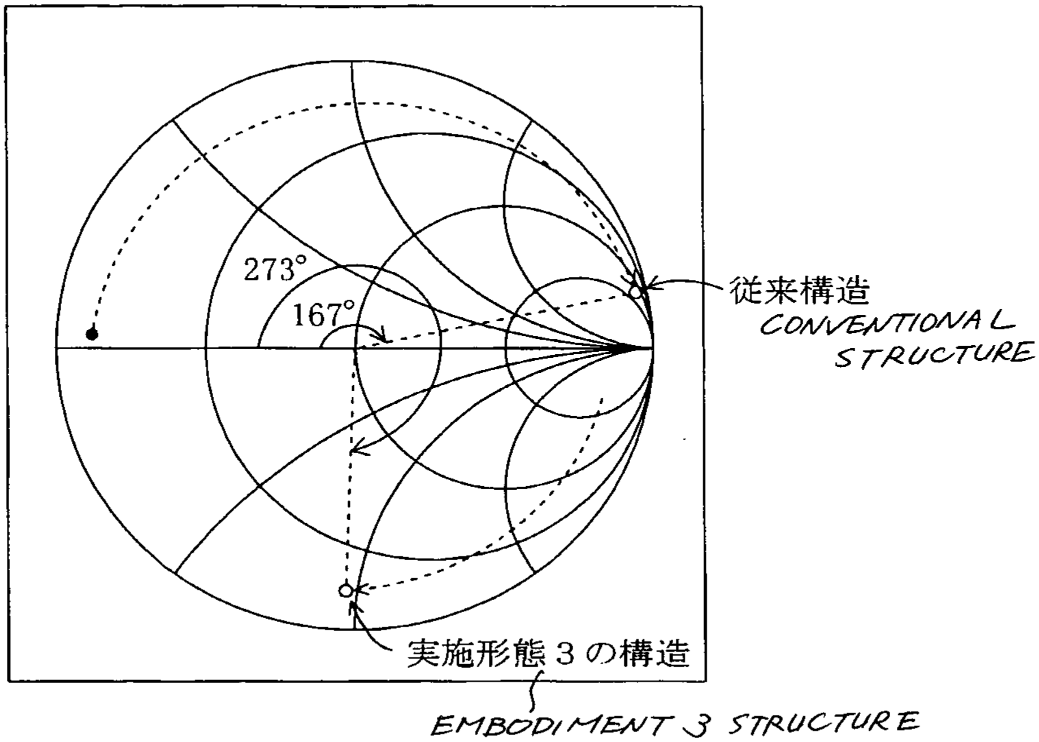
【図７】
[Fig. 7]



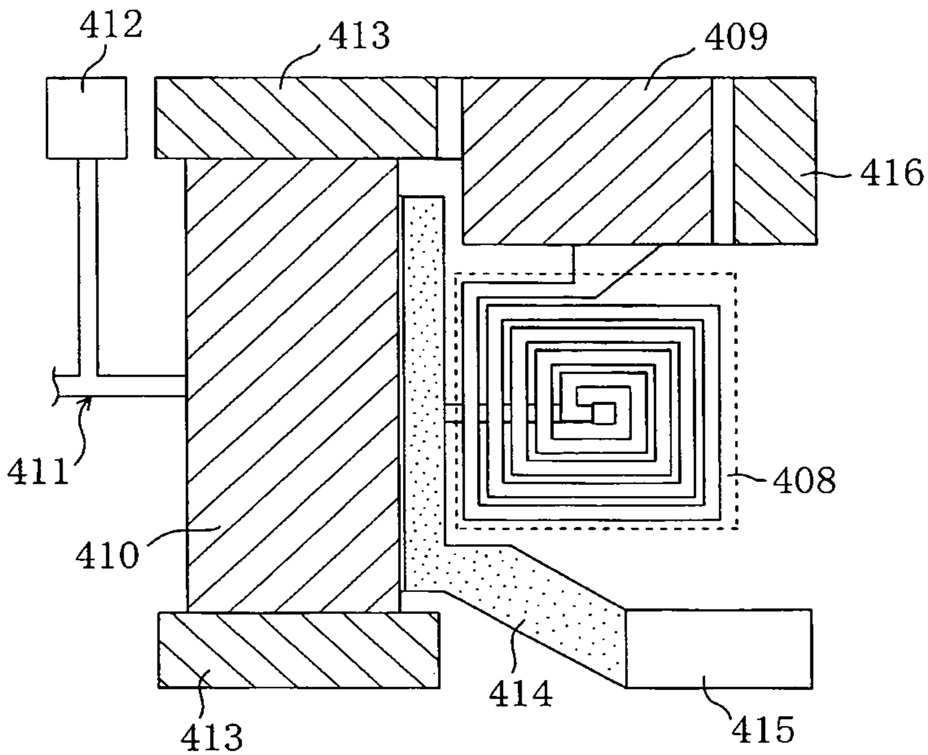
【図８】
[Fig. 8]



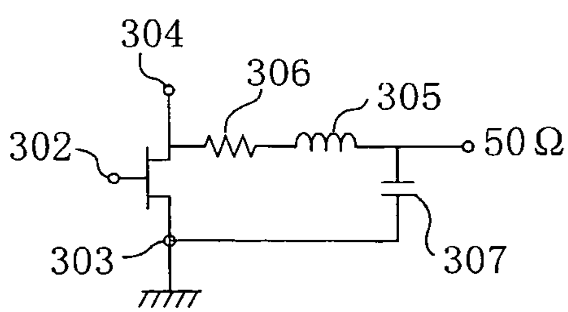
【図９】
[Fig. 9]


273°
167°
従来構造
CONVENTIONAL STRUCTURE
実施形態３の構造
EMBODIMENT 3 STRUCTURE

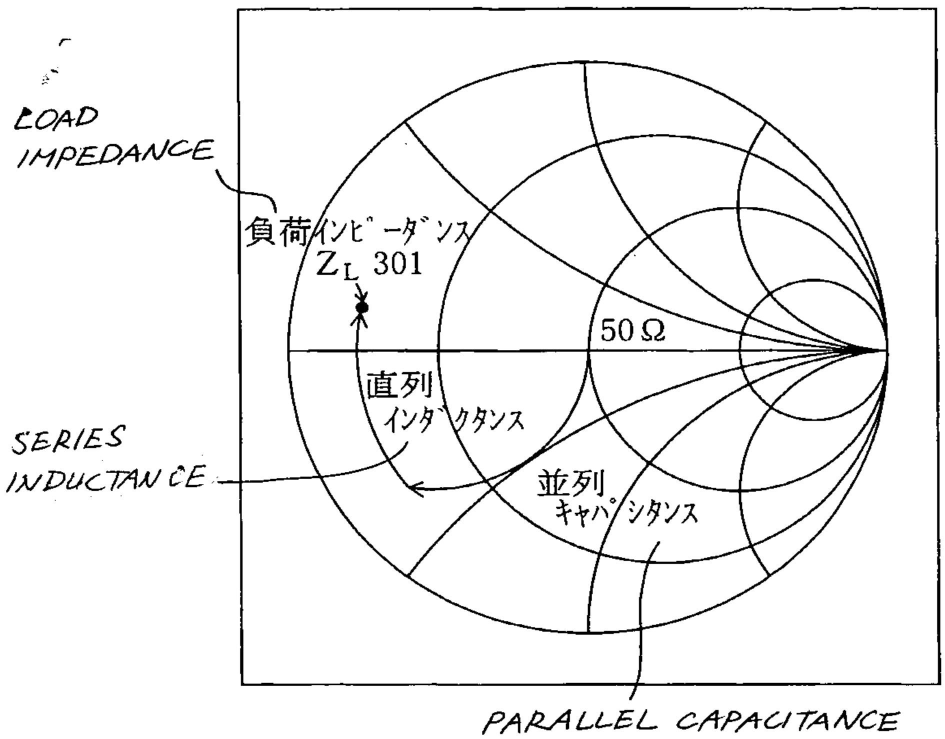
【図１０】
[Fig. 10]



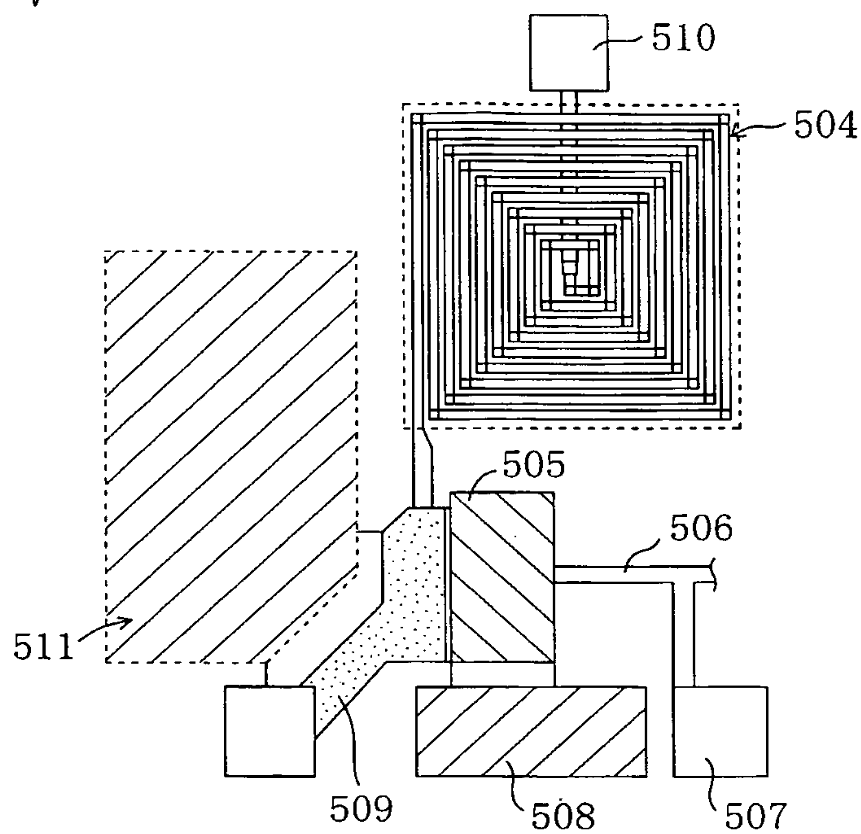
【図１１】
[Fig. 11]



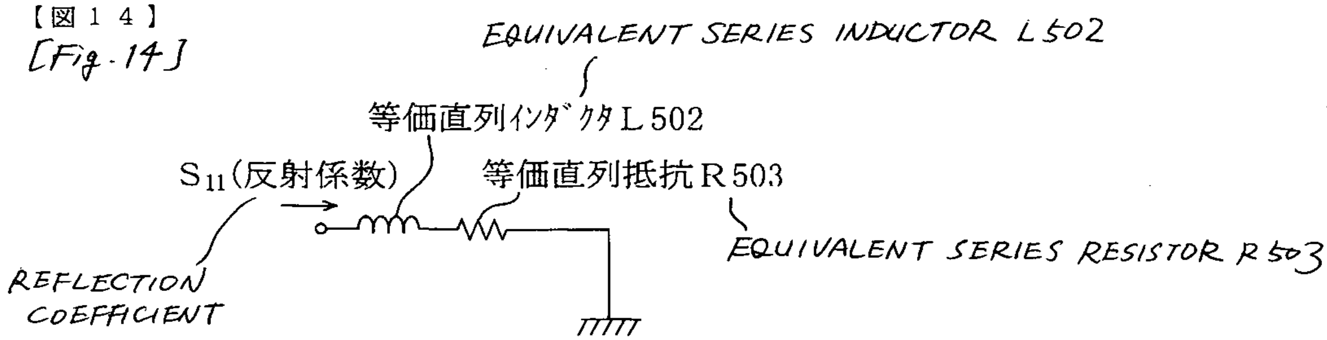
【図１２】
[Fig. 12]


LOAD IMPEDANCE
負荷インピーダンス
Z_L 301
50 Ω
直列インダクタンス
SERIES INDUCTANCE
並列キャパシタンス
PARALLEL CAPACITANCE

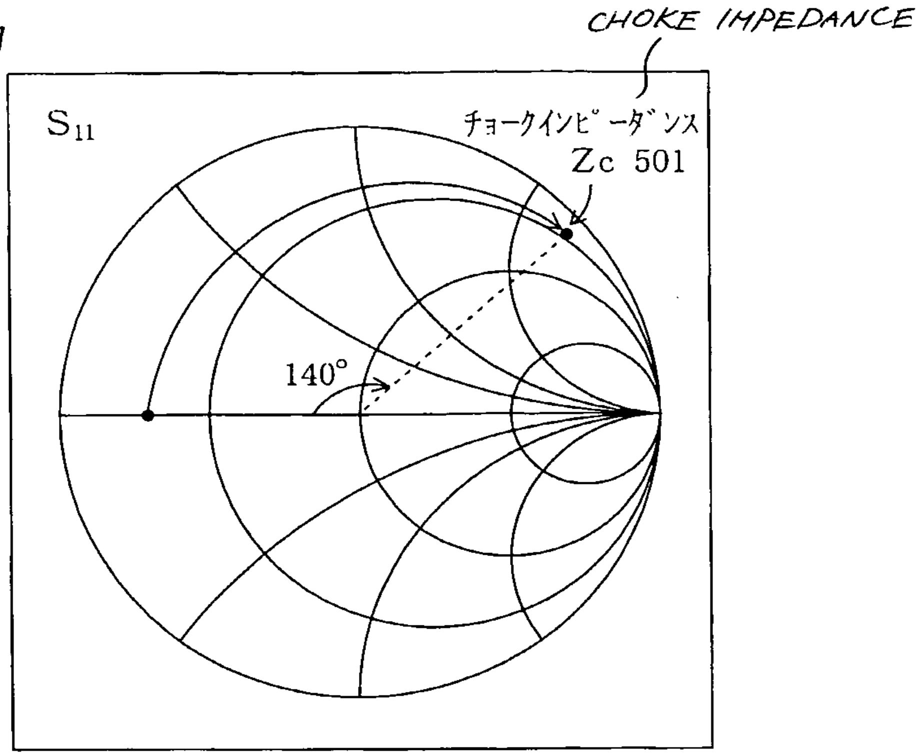
【図１３】
[Fig. 13]



【図１４】
[Fig. 14]



【図１５】
[Fig. 15]



【図１６】
[Fig. 16]